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L3	L1 and (diode or transistor)	28	L3
L2	L1 and (diode near5 transistor)	3	L2
L1	detect$3 near5 (hot or live) near5 (swap$4 or insert$3)	75	L1

END OF SEARCH HISTORY

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Terms	Documents
L3	0

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DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L1 and (diode or transistor)	28	L3
L2	L1 and (diode near5 transistor)	3	L2
L1	detect$3 near5 (hot or live) near5 (swap$4 or insert$3)	75	L1

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Refine Search

Search Results -

Terms	Documents
(439/620 |327/562 |361/679 |361/686 |710/301 |710/302 |710/303 |710/304 |710/2 |323/908 |326/87).ccls.	4322

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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L1	710/301-304,2;326/87;323/908;327/562;361/679,686;439/620.ccls.	4322	L1

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Refine Search

Search Results -

Terms	Documents
L1 and L2	31

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- US Patents Full-Text Database
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- EPO Abstracts Database
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	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	l1 and L2	31	L3
L2	detect$3 near10 (hot or live) near10 (swap$4 or insert$3)	142	L2
L1	710/301-304,2;326/87;323/908;327/562;361/679,686;439/620.ccls.	4322	L1

END OF SEARCH HISTORY

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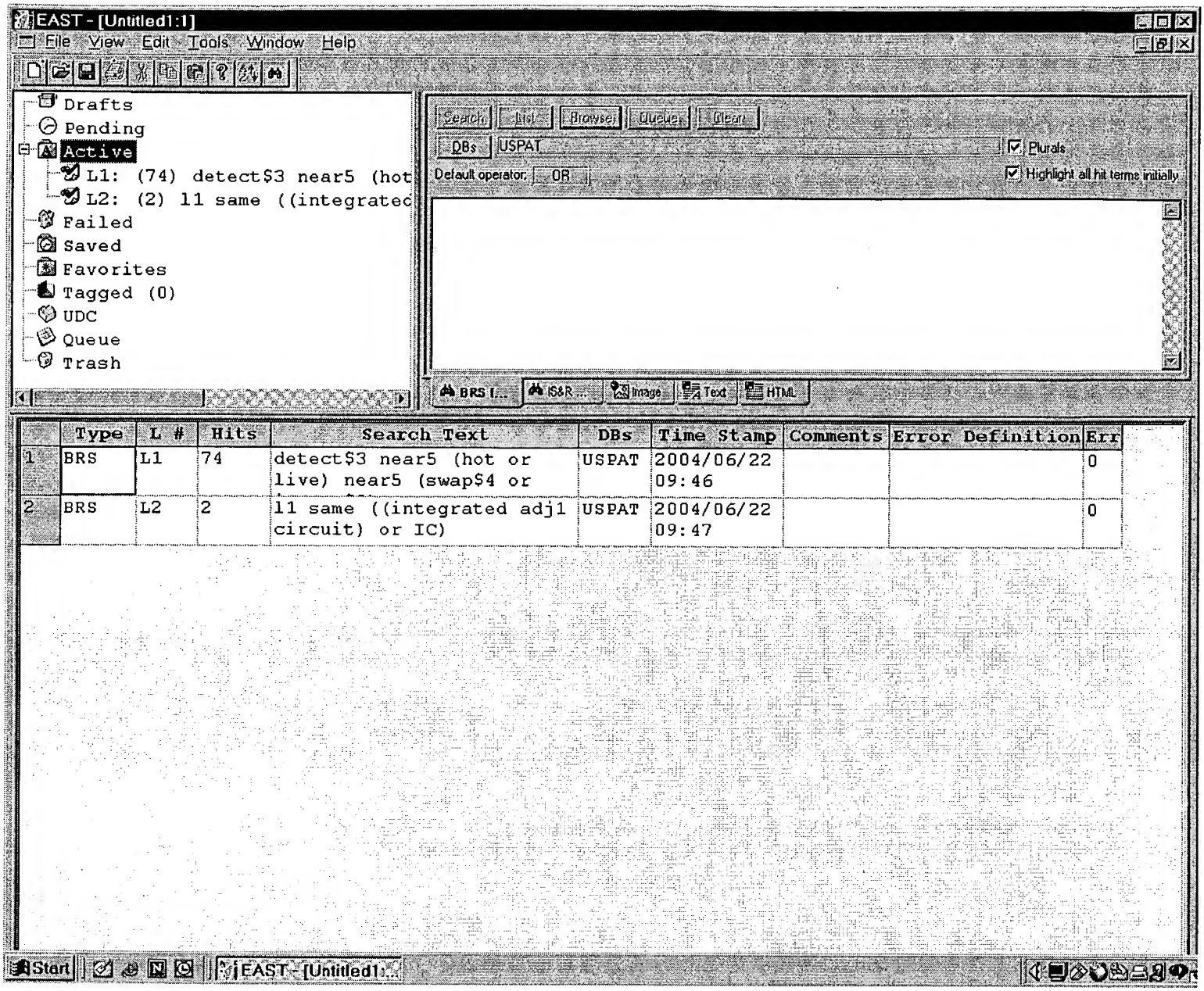

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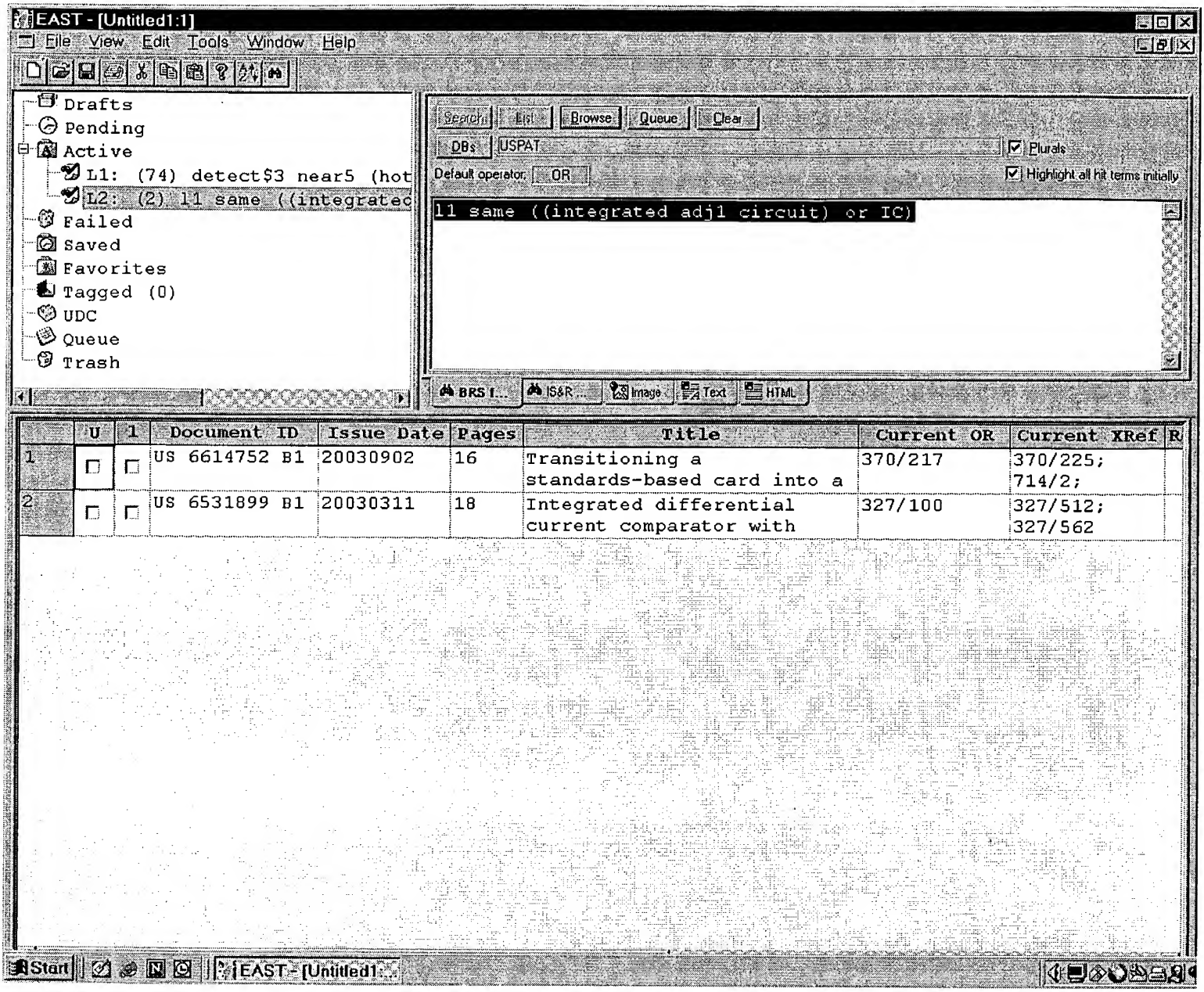
1	BRS	L1	74	detect$3 near5 (hot or live) near5 (swap$4 or	USPAT	2004/06/22 09:46			0
2	BRS	L2	2	l1 same ((integrated adj1 circuit) or IC)	USPAT	2004/06/22 09:47			0


EAST - [Untitled1:1]
File View Edit Tools Window Help
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L1: (74) detect$3 near5 (hot
L2: (2) l1 same ((integrated
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Plurals
Default operator:
OR
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l1 same ((integrated adj1 circuit) or IC)
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US 6614752 B1
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16
Transitioning a standards-based card into a
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370/225; 714/2;
2
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18
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1 **Annotation of video by alignment to reference imagery**
Hanna, K.J.; Sawhney, H.S.; Kumar, R.; Guo, Y.; Samarasekara, S.;
Multimedia Computing and Systems, 1999. IEEE International Conference on , Volume: 1 , 7-11 June 1999
Pages:38 - 43 vol.1

[Abstract] [PDF Full-Text (644 KB)] **IEEE CNF**

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2 **Tactile sensor using piezoelectric resonator**
Maezawa, M.; Imahashi, T.; Kuroda, Y.; Adachi, H.; Yanagisawa, K.;
Solid State Sensors and Actuators, 1997. TRANSDUCERS '97 Chicago., 1997 International Conference on , Volume: 1 , 16-19 June 1997
Pages:117 - 120 vol.1

[Abstract] [PDF Full-Text (364 KB)] **IEEE CNF**

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3 **Simulating respiratory motion in whole-body PET imaging with the phantom**
Isoardi, R.A.; Comtat, C.; Frouin, V.; Delzescaux, T.; Trebossen, R.;
Nuclear Science Symposium Conference Record, 2002 IEEE , Volume: 2 , 10-Nov. 2002
Pages:1113 - 1115 vol.2

[Abstract] [PDF Full-Text (442 KB)] **IEEE CNF**

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4 **Development of a high resolution, 2D detector system for iodine-13 scintigraphy**
Sonnenberg, F.; Bussmann, N.; Engels, R.; Reinartz, R.; Schramm, N.; Fried W.; Langen, K.-J.; Halling, H.;
Nuclear Science Symposium, 1999. Conference Record. 1999 IEEE , Volume:

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3 , 24-30 Oct. 1999
Pages:1173 - 1175 vol.3

[Abstract] [PDF Full-Text (336 KB)] **IEEE CNF**

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1 **Electrical phenomena during Hot Swap events**
Trinitis, C.; Karl, W.; Leberecht, M.;
Dependable Computing, 2000. Proceedings. 2000 Pacific Rim International Symposium on , 18-20 Dec. 2000
Pages:19 - 26

[Abstract] [PDF Full-Text (560 KB)] **IEEE CNF**

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2 **AMP Z-pack 2 mm HM connectors with quiet mate contacts for resol of nanosecond discontinuity in hot-swap applications**
Demirci, H.H.; Laub, M.; Fry, C.;
Electronic Components and Technology Conference, 2001. Proceedings., 51st May-1 June 2001
Pages:1239 - 1244

[Abstract] [PDF Full-Text (668 KB)] **IEEE CNF**

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3 **Solutions for hot-swap problem in parallel low output voltage AC/D converters with multiple outputs**
Lei Hua; Shiguo Luo; Batarseh, I.;
Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 20 Midwest Symposium on , Volume: 2 , 14-17 Aug. 2001
Pages:980 - 983 vol.2

[Abstract] [PDF Full-Text (159 KB)] **IEEE CNF**

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4 **Runtime software reorganization by traditional OS features**
Nagamatsu, L.;
Principles of Software Evolution, 2000. Proceedings. International Symposium on , 1-2 Nov 2000

Pages:311 - 315

[Abstract] [PDF Full-Text (356 KB)] IEEE CNF

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5 **Hybrid battery system for a pocket computer**
Hamburgen, W.;
Battery Conference on Applications and Advances, 2002. The Seventeenth Annual , 15-18 Jan. 2002
Pages:227

[Abstract] [PDF Full-Text (38 KB)] IEEE CNF

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6 **Experimental research on a hot swappable bus system**
Yamada, T.; Kaminaga, Y.; Kurosawa, K.; Ohashi, A.; Masui, K.;
American Control Conference, 1997. Proceedings of the 1997 , Volume: 1 , 4 June 1997
Pages:213 - 217 vol.1

[Abstract] [PDF Full-Text (500 KB)] IEEE CNF

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7 **Dynamic hardware plugins in an FPGA with partial run-time reconfiguration**
Horta, E.L.; Lockwood, J.W.; Taylor, D.E.; Parlour, D.;
Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002
Pages:343 - 348

[Abstract] [PDF Full-Text (782 KB)] IEEE CNF

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8 **A framework for live software upgrade**
Lizhou Yu; Shoja, G.C.; Muller, H.A.; Srinivasan, A.;
Software Reliability Engineering, 2002. ISSRE 2002. Proceedings. 13th International Symposium on , 12-15 Nov. 2002
Pages:149 - 158

[Abstract] [PDF Full-Text (1938 KB)] IEEE CNF

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9 **Supporting hot-swappable components for system software**
Hui, K.; Appavoo, J.; Wisniewski, R.; Auslander, M.; Edelsohn, D.; Gamsa, B. Krieger, O.; Rosenburg, B.; Stumm, M.;
Hot Topics in Operating Systems, 2001. Proceedings of the Eighth Workshop on , 20-22 May 2001
Pages:170

[Abstract] [PDF Full-Text (209 KB)] IEEE CNF

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10 **A high power linear solid state pulser**
Yen, B.; Davis, B.; Booth, R.;
Particle Accelerator Conference, 1999. Proceedings of the 1999 , Volume: 3 , March-2 April 1999
Pages:1506 - 1508 vol.3

[Abstract] [PDF Full-Text (335 KB)] IEEE CNF

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11 **Practical case study of remote and local powering system for hybri fibre-coaxial (HFC) networks**

Alvarez, E.; Ruiz, F.M.; Corral, J.; Manso, J.; Bustos, D.; Martin, F.; Fornis, A

Telecommunications Energy Conference, 2001. INTELEC 2001. Twenty-Third International , 14-18 Oct. 2001

Pages:294 - 300

[Abstract] [PDF Full-Text (947 KB)] **IEE CNF**

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1 **Experimental research on a hot swappable bus system**
Yamada, T.; Kaminaga, Y.; Kurosawa, K.; Ohashi, A.; Masui, K.;
American Control Conference, 1997. Proceedings of the 1997 , Volume: 1 , 4 June 1997
Pages:213 - 217 vol.1

[Abstract] [PDF Full-Text (500 KB)] **IEEE CNF**

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2 **Dynamic hardware plugins in an FPGA with partial run-time reconfiguration**
Horta, E.L.; Lockwood, J.W.; Taylor, D.E.; Parlour, D.;
Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002
Pages:343 - 348

[Abstract] [PDF Full-Text (782 KB)] **IEEE CNF**

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Experimental research on a hot swappable bus system

Yamada, T. Kaminaga, Y. Kurosawa, K. Ohashi, A. Masui, K.
Res. Lab., Hitachi Ltd., Ibaraki, Japan ;

This paper appears in: **American Control Conference, 1997. Proceedings of the 1997**

Meeting Date: 06/04/1997 - 06/06/1997
Publication Date: 4-6 June 1997
Location: Albuquerque, NM USA
On page(s): 213 - 217 vol.1
Volume: 1
Reference Cited: 11
Number of Pages: 6 vol. (lix+xi+xvii+xii+xvii+xii+3994)
Inspec Accession Number: 6010491

Abstract:
For industrial controllers, **hot swap** capability is needed to increase system availability, as well as supplying many slots. Based on a PCI bus, we developed a new system bus where we can utilize commercially available chips for expansion modules. We use the MOS transfer logic switch near the system bus to reduce the stub length. We report the calculated and experimental results on the performance of this system bus

Index Terms:

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MOS **integrated circuits** controllers industrial control integrated logic circuits modules peripheral interfaces switches system buses MOS transfer logic switch PCI bus expansion modules hot swappable bus system industrial controllers stub length system availability

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Dynamic hardware plugins in an FPGA with partial run-time reconfiguration

Horta, E.L. Lockwood, J.W. Taylor, D.E. Parlour, D.
Escola Politecnica, Sao Paulo Univ., Brazil

This paper appears in: **Design Automation Conference, 2002. Proceedings. 39th**

Publication Date: 10-14 June 2002
On page(s): 343 - 348
ISSN: 0738-100X
Number of Pages: xxxvi+919
Inspec Accession Number: 7461250

Abstract:
Tools and a design methodology have been developed to support partial run-time reconfiguration of FPGA logic on the Field Programmable Port Extender. High-speed Internet packet processing circuits on this platform are implemented as Dynamic Hardware Plugin (DHP) modules that fit within a specific region of an FPGA device. The PARBIT tool has been developed to transform and restructure bitfiles created by standard computer aided design tools into partial bitsteams that program DHPs. The methodology allows the platform to **hot-swap** application-specific DHP modules without disturbing the operation of the rest of the system.

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Index Terms:

field programmable gate arrays **integrated circuit** layout logic CAD network routing reconfigurable architectures FPGA PARBIT tool application-specific DHP modules bitfile restructuring bitfile transformation computer aided design tools design methodology dynamic hardware plugins field programmable port extender high-speed Internet packet processing circuits hot swapping partial bitsteams partial run-time reconfiguration

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☐ 1. Document ID: US 5844759 A

Using default format because multiple data bases are involved.

L2: Entry 1 of 3 File: USPT Dec 1, 1998

US-PAT-NO: 5844759
DOCUMENT-IDENTIFIER: US 5844759 A

TITLE: Electrical fault interrupter

DATE-ISSUED: December 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hirsh; Stanley S.	El Paso	TX		
Nemir; David C.	El Paso	TX	79902	

US-CL-CURRENT: 361/42; 361/103, 361/49

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 2. Document ID: US 5764926 A

L2: Entry 2 of 3 File: USPT Jun 9, 1998

US-PAT-NO: 5764926
DOCUMENT-IDENTIFIER: US 5764926 A

TITLE: Supressing in rush current from a power supply during live wire insertion and removal of a circuit board

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 3. Document ID: US 3304432 A

L2: Entry 3 of 3 File: USOC Feb 14, 1967

US-PAT-NO: 3304432
DOCUMENT-IDENTIFIER: US 3304432 A

TITLE: Photosensitive sensing system for a currency detector

h e b b g e e e f e b ef b e

DATE-ISSUED: February 14, 1967

INVENTOR-NAME: LEINGANG FRANK A; COUSINS WILLIAM R

US-CL-CURRENT: 250/556, 209/534, 250/214R

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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L3: Entry 5 of 28 File: USPT Sep 23, 2003

US-PAT-NO: 6625681
DOCUMENT-IDENTIFIER: US 6625681 B1

TITLE: State activated one shot with extended pulse timing for hot-swap applications

DATE-ISSUED: September 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Erickson; Michael John	Loveland	CO		
Brush; Richard K.	Los Altos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, L.P.	Houston	TX			02

APPL-NO: 09/ 272798 [PALM]
DATE FILED: March 29, 1999

INT-CL: [07] G06 F 36/61, G06 F 13/00, G06 F 7/10

US-CL-ISSUED: 710/302; 710/58, 710/330, 710/301, 710/303
US-CL-CURRENT: 710/302; 710/301, 710/303, 710/58

FIELD-OF-SEARCH: 710/302, 710/58, 710/330, 710/301, 710/303

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4245270	January 1981	Busby	361/58
☐	4886984	December 1989	Nakaoka	327/143
☐	5317697	May 1994	Husak et al.	395/325
☐	5604873	February 1997	Fite et al.	395/283
☐	5754797	May 1998	Takahashi	710/302
☐	5758102	May 1998	Carey et al.	710/302
	5862393	January 1999	Davis	710/302

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☐	5922060	July 1999	Goodrum	710/302
☐	5938771	August 1999	Williams et al.	713/310
☐	6274949	August 2001	Lioux et al.	307/64

ART-UNIT: 2189

PRIMARY-EXAMINER: Vo; Tim

ABSTRACT:

An apparatus and method for indicating and allowing hot swapping of a circuit board. During both insertion and extraction of a circuit board from a system, two inputs signals are generated from staggered pins located on the circuit board's connector. The inputs are processed through a NAND function implemented with transistors and output to two Schmitt trigger inverters connected in series. The output of the series connection of Schmitt trigger inverters goes high when both input signals are high and goes low when one of the inputs signals goes low. In addition, through the use of a resistor, capacitor combination connected to the input of the first Schmitt trigger inverter, the output signal remains high for a period of time after one of the input signals goes low. This additional period of time prevents any damage or disruption of signaling caused by transient current and voltage fluctuations as a circuit board is inserted or extracted. The output signal can be used in both single-ended and differential SCSI applications.

9 Claims, 6 Drawing figures

L3: Entry 16 of 28 File: USPT Jun 4, 2002

DOCUMENT-IDENTIFIER: US 6401157 B1
TITLE: Hot-pluggable component detection logic

Abstract Text (1):
A computer system having detection logic for detecting a hot-pluggable component module being added to the computer system. The detection logic determines when the hot-pluggable component module is fully inserted in a component connector, waits a predetermined time to insure that the hot-pluggable component module is properly seated in and electrical connections made to the component connector, and then notifies a hot-plug controller that a new component module is available for use in the computer system. The hot-pluggable component module, such as a memory module, may be used by the computer system as a replacement for a defective module, upgrade and/or addition without disturbing normal operation of the computer system.

Brief Summary Text (14):
The RAM module connectors or memory connectors are electrically isolated from the computer system memory bus with field effect transistor (FET) signal isolation buffers interposed between the connector signal pins and a memory controller. Power FET switches are interposed between the connector power pins and the computer system power buses. Each memory connector may also contain one or more software and/or hardware controllable light emitting diodes (LEDs) of various colors (electronically controllable) to indicate the status of the corresponding memory connector. Control and sense logic is implemented to control operation of the PET signal isolation buffers between the system memory controller and the memory connectors, the power FET switches between the computer system power bus(es) and the memory connectors, and LED status indication. This control and sense logic may monitor ("snoop") memory bus activity so that a memory connector may be connected to or disconnected from the memory bus when the memory bus in inactive, i.e., no read or write operations. The control and sense logic initiates connection of the memory connector/added RAM module when the hot-plug detection logic signals at the added RAM module is present in the connector. Integration and operation of the hot-plug component modules is more fully described in commonly owned U.S. patent application Ser. No. 09/303,369; filed Apr. 30, 1999; entitled "Replacement, Upgrade, and/or Addition of Hot-Pluggable Components in a Computer System" by Theodore F. Emeron, Vincent Nguyen Peter Michels and Steve Clohset, and is hereby incorporated by reference herein.

Detailed Description Text (10):
Electronic signal isolation buffers such as field effect transistors (FETs) 160, and power switches such as power FET switches 162 are interposed between each of the hot-pluggable connectors 402 (see FIG. 4), the memory buses 105a and 105b, and the computer system power, respectively. Also on the same printed circuit board is a hot-plug controller 164 which comprises control and timing logic used to control the operation of the FET signal isolation buffers 160 and power FET switches 162, and determine when a RAM 106 module is plugged into or removed from its associated connector 402. The hot-plug controller 164 also may determine whether the correct number of RAM 106 modules are plugged into the connectors 402. The hot-plug controller 164 may further be used to control the connection and disconnection of the hot-pluggable connectors 402 (see FIG. 4) from the memory controller 204 (see FIG. 2) in a synchronous fashion, i.e., powering up of the new RAM 106 module with

the power FET switches 162 so that the new module circuits become stabilized and initialized, then connecting the new RAM 106 module in the connector 402 with the FET signal isolation buffers 160 to the memory bus 105a only when the memory bus 105a is inactive (no address and/or data being asserted). For the failing RAM 106 module, the memory bus 105a is disconnected during an inactive time by the FET signal isolation buffers 160, and then the power is disconnected from the connector 402 by the power FET switches 162. The hot plug controller 164 a receives signal(s) from detection logic 166 which indicates that a new RAM 106 module has been plugged into the connector 402. The detection logic 166 determines that the new RAM 106 module has been plugged into the connector 402 by monitoring a pin connection which changes its resistance, voltage or current value after the RAM 106 module is plugged therein. The detection logic 166 waits a certain period of time to insure that the RAM 106 module is properly seated in the connector 402.

Detailed Description Text (15):
When the RAM 106 module is detected as being plugged into the connector 402, the detection logic signals the hot-plug controller 164 after a period of time has elapsed so as to insure that the RAM 106 module is properly seated in the connector 402. Then the hot-plug controller 164 causes the power FET switches 162 to connect the power pins of the connector 402 to the computer system power bus (not illustrated), and, after the circuits of the RAM 106 module have had time to stabilize, the FET signal isolation buffers 160 connect the memory controller address, control and data bus 105a to the signal pins of the connector 402. Light emitting diode (LED) 404 indicators may be strategically located next to their associated connectors 402 for indication of status and operation thereof, and any RAM 106 module plugged therein. The hot-plug controller 164 may control the LEDs 404, and may also have circuits for snooping the memory bus 105a for memory read and write activities.

Detailed Description Text (18):
The connector 402 has three pins 504a, 504b and 504c that are adapted for connection to the edge connector 506 pins 502a, 502b and 502c. Pin 504c is connected to a system ground 514. The cathodes of diodes 512a and 512b are connected to pins 504a and 504b, respectively. Capacitors 524a and 524b also are connected to the pins 504a and 504b, respectively, and may be used to bypass these pins effectively to ground at alternating current operating frequencies. The anodes of diodes 512a and 512b are connected to first ends of pull up resistors 516a and 516b, respectively, and to inputs of the OR gate 518. The other ends of the pull up resistors 516a and 516b are connected to system logic voltage Vcc. When both of the cathodes of diodes 512a and 512b are connected to ground by the pins 504a and 504b, respectively, the inputs to the OR gate 518 will be substantially pulled to ground level, or a logic low, and the output of the OR gate 518 will then be at a logic low. If either or both of the inputs of the OR gate 518 are pulled to Vcc by pull up resistors 516a and 516b (one or both of the diodes 512a and 512b cathodes are not connected to ground), then the output of the OR gate 518 will be at a logic high.

CLAIMS:

3. The computer system of claim 1, wherein said plurality of component bus switches comprise a plurality of field effect transistor switches.

4. The computer system of claim 1, wherein said plurality of component power switches comprise a plurality of field effect transistor power switches.

17. The computer system of claim 15, further comprising a plurality of diodes connected between the plurality of inputs of said OR gate and the respective ones of the plurality of pins of the one of said plurality of component connectors.

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L3: Entry 16 of 28 File: USPT Jun 4, 2002

US-PAT-NO: 6401157
DOCUMENT-IDENTIFIER: US 6401157 B1

TITLE: Hot-pluggable component detection logic

DATE-ISSUED: June 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nguyen; Vincent	Sugarland	TX		
Emerson; Theodore F.	Houston	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Compaq Information Technologies Group, L.P.	Houston	TX			02

APPL-NO: 09/ 303180 [PALM]
DATE FILED: April 30, 1999

PARENT-CASE:
CROSS REFERENCE TO RELATED PATENT APPLICATION This patent application is related to commonly owned U.S. patent application Ser. No. 09/303,369; filed Apr. 30, 1999; entitled "Replacement, Upgrade, and/or Addition of Hot-Pluggable Components in a Computer System" by Theodore F. Emerson, Vincent Nguyen Peter Michels and Steve Clohset, and is hereby incorporated by reference for all purpose.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/302; 711/115
US-CL-CURRENT: 710/302; 711/115

FIELD-OF-SEARCH: 710/100-304, 361/679-686, 711/115

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5530302	June 1996	Hamre et al.	307/147
☐	5584030	December 1996	Husak et al.	713/300
	5754797	May 1998	Takahashi	710/103

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☐				
☐	5758102	May 1998	Carey et al.	710/103
☐	5781744	July 1998	Johnson et al.	710/103
☐	5881251	March 1999	Fung et al.	710/103
☐	5886431	March 1999	Rutigliano	307/131
☐	5943482	August 1999	Culley et al.	361/798
☐	5951660	September 1999	Wonterghem	710/103
☐	6044424	March 2000	Amin	710/103
☐	6047343	April 2000	Olarig	710/102
☐	6062480	May 2000	Evoy	235/492
☐	6115766	September 2000	Bailis	710/103
☐	6131134	October 2000	Huang et al.	710/103
☐	6141711	October 2000	Shah et al.	710/103

ART-UNIT: 2181

PRIMARY-EXAMINER: Lefkowitz; Sumati

ATTY-AGENT-FIRM: Conley, Rose & Tayon, P.C.

ABSTRACT:

A computer system having detection logic for detecting a hot-pluggable component module being added to the computer system. The detection logic determines when the hot-pluggable component module is fully inserted in a component connector, waits a predetermined time to insure that the hot-pluggable component module is properly seated in and electrical connections made to the component connector, and then notifies a hot-plug controller that a new component module is available for use in the computer system. The hot-pluggable component module, such as a memory module, may be used by the computer system as a replacement for a defective module, upgrade and/or addition without disturbing normal operation of the computer system.

20 Claims, 5 Drawing figures

L3: Entry 17 of 28 File: USPT Sep 4, 2001

DOCUMENT-IDENTIFIER: US 6286066 B1
TITLE: Hot-plug interface for detecting adapter card insertion and removal

Detailed Description Text (9):
The controller 222 has monitoring connections to the electrically-conductive flip-down retainer 210 at electrical contacts 228. The controller 222 is connected to the electrically-conductive flip-down retainer 210 to sense and monitor engagement and disengagement of the adapter card 212 with the adapter card slot 214. The controller 222 also includes control connections to the adapter card slot 214 including a connection to a switch 230, such as a field-effect transistor (FET) switch, that controls application of power to the adapter card slot 214. The computer system 200 also has a control connection to an indicator 232, such as a light-emitting diode (LED), that indicates whether power is applied to the adapter card slot 214.

First Hit Fwd Refs

Generate Collection Print

L3: Entry 17 of 28 File: USPT Sep 4, 2001

US-PAT-NO: 6286066
DOCUMENT-IDENTIFIER: US 6286066 B1

TITLE: Hot-plug interface for detecting adapter card insertion and removal

DATE-ISSUED: September 4, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hayes; Stuart	Austin	TX		
Khatri; Mukund P.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dell U.S.A., L.P.	Round Rock	TX			02

APPL-NO: 09/ 211321 [PALM]
DATE FILED: December 15, 1998

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/103; 710/102, 235/492
US-CL-CURRENT: 710/302; 235/492

FIELD-OF-SEARCH: 710/101-103, 710/8, 710/2, 710/10, 710/15, 710/16, 710/18, 235/492, 235/472.01, 235/441, 235/487

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4365317	December 1982	Gheewala	
☐	4494329	January 1985	Post et al.	
☐	4787060	November 1988	Boudreau et al.	
☐	5062806	November 1991	Ohno et al.	
☐	5241643	August 1993	Durkin et al.	
☐	5601349	February 1997	Holt	
☐	5742013	April 1998	Myojin et al.	

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☐	5881251	March 1999	Fung et al.	710/103
☐	5996035	November 1999	Allen et al.	710/103
☐	6026458	February 2000	Rasums	710/103
☐	6032209	February 2000	Mros et al.	710/103
☐	6038615	March 2000	Yamada et al.	710/2
☐	6044424	March 2000	Amin	710/103
☐	6062480	May 2000	Evoy	235/492

OTHER PUBLICATIONS

"PCI Bus Hot Plug Specification", Revision 1.0, Jun. 15, 1997, pp. i-vi, and 1-29.

ART-UNIT: 211

PRIMARY-EXAMINER: Beausoleil; Robert

ASSISTANT-EXAMINER: Phan; Raymond N

ATTY-AGENT-FIRM: Skjerven Morrill MacPherson LLP Koestner; Ken J.

ABSTRACT:

Adapter cards generally have a metal bracket at one end. The adapter card attaches to an adapter card slot of a computer system by fastening the bracket to a connector on the computer system. Conventionally, the bracket is fastened to the connector using a screw. It has been discovered that an electrically-conductive flip-down retainer advantageously functions as an improved fastener to secure the adapter card to the connector. The electrically-conductive flip-down retainer is a single structure that performs the combined functions of an electrical switch and a mechanical fastener. The electrically-conductive flip-down retainer includes electrical contacts that form a closed circuit when the bracket is fastened to the connector and an open circuit when the bracket is not fastened. The electrical contacts are connected to conductors extending to a controller. The controller monitors the status of the electrical switch of the electrically-conductive flip-down retainer and controls application of power to the adapter card slot, typically under control of an operating system. The controller terminates power to the adapter card slot when the electrically-conductive flip-down retainer is unfastened, indicating that the adapter card is disengaged from the adapter card slot. The controller restores power to the adapter card slot when the electrically-conductive flip-down retainer is fastened, indicating the adapter card is engaged with the adapter card slot.

26 Claims, 11 Drawing figures

First Hit Fwd Refs

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L3: Entry 22 of 28 File: USPT Jun 9, 1998

US-PAT-NO: 5764926
DOCUMENT-IDENTIFIER: US 5764926 A

TITLE: Supressing in rush current from a power supply during live wire insertion and removal of a circuit board

DATE-ISSUED: June 9, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fukuda; Kimio	Ebina			JP
Morita; Kazuo	Hadano			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 08/ 423214 [PALM]
DATE FILED: April 17, 1995

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	6-082870	April 21, 1994

INT-CL: [06] H02 H 9/00

US-CL-ISSUED: 395/283; 361/58, 323/908
US-CL-CURRENT: 710/302; 323/908, 361/58

FIELD-OF-SEARCH: 395/283, 395/281, 395/750, 365/226, 365/228, 365/229, 327/545, 327/549, 327/566, 327/380, 327/381, 361/58, 323/908

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4725741	February 1988	Shekhaiwat et al.	327/575
☐	4734595	March 1988	Le Roux et al.	327/575
☐	4977341	December 1990	Stein	327/380

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☐	5132564	July 1992	Fletcher et al.	307/443
☐	5317697	May 1994	Husak et al.	395/283
☐	5323291	June 1994	Boyle et al.	361/683
☐	5369593	November 1994	Papamarcos et al.	364/488
☐	5430404	July 1995	Campbell et al.	327/566

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
558770	September 1993	EP	
3-171214	July 1991	JP	
5-289788	November 1993	JP	
2248352	April 1992	GB	

ART-UNIT: 235

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Lefkowitz; Sumati

ATTY-AGENT-FIRM: Fay, Sharpe, Beall, Fagan, Minnich & McKee

ABSTRACT:

A circuit unit to be inserted or removed by live wire work into or from a system having a plurality of circuit units and a power source to supply power to the plurality of circuit units includes a first circuit to supply power to the circuit unit from the power source when the circuit unit is inserted into the system; and a second circuit to supply power to the circuit unit in normal operation after the circuit unit is inserted into the system. The first circuit nearly stops supplying power about the time when the second circuit starts supplying power and by this arrangement, it becomes possible to vary the timing of inrush currents attending on a supply of power from a plurality of power sources. A removal permission indicator can be installed which can be turned on by a voltage supplied from the power source under a condition that permission to remove the unit has been issued. In order to adjust the unit inserting speed, a lever is mounted rotatably at one end of each circuit unit, for multiplying a force for removing said unit by using as a point of force application a certain point in said system under the condition that permission to remove the circuit unit has been issued. A connector of the circuit unit is structured so as to be freely movable at a mounting portion for several millimeters on the surface of a metal sheet when the system and the connector of the unit are connected mechanically and electrically.

35 Claims, 14 Drawing figures

L3: Entry 23 of 28 File: USPT Apr 1, 1997

DOCUMENT-IDENTIFIER: US 5617081 A
**** See image for Certificate of Correction ****
TITLE: Method and apparatus for live insertion and removal of electronic sub-assemblies

Brief Summary Text (7):
An additional consideration that arises when insertion or removal of a sub-assembly to or from a powered assembly is desirable, is protection of the circuitry on the sub-assembly being inserted or removed. Many integrated circuits are fabricated such that there is a low impedance path between a circuit output and Vcc in a back biased direction. When such a circuit is present on a sub-assembly that is inserted into a live assembly, current from the live assembly, seeking the path of least resistance, will surge through the low impedance path possibly destroying the device. Some integrated circuit manufacturers put a diode in the low impedance path in certain logic families. However, often these diodes are not tested and one cannot be certain of their presence or functionality.

Brief Summary Text (12):
As presently disclosed, an active switching device such as a metal oxide semiconductor field effect transistor (mosfet) and related massive circuitry, and a connector having a plurality of graduated pin lengths effect a controlled ramp-up and ramp-down of power to a sub-assembly inserted into and removed from a live electronic assembly. During insertion of an unpowered sub-assembly into a live electronic assembly, a first set of contact pins (long pins) provide a ground and a preliminary voltage (PRE.sub.-- VCC) to the inserted sub-assembly to power live insertion request logic. A live insertion period request is issued which causes a system bus arbiter to force the system bus to an idle state after any bus operation in progress is completed. A second set of contact pins (medium pins) provide power to the mosfet and related passive circuitry which ramps up power to the inserted sub-assembly assuring that current in-rush is gradual. A third set of contact pins (short pins) bypass the mosfet circuitry and indicate when the sub-assembly is fully inserted. During removal short pins disengage first. The mosfet bypass is removed. An indication is issued that the sub-assembly is not fully seated. A live insertion period is requested. The mosfet and related passive circuitry ramp down power after the medium pins disengage until the power to the sub-assembly is completely removed upon full withdrawal.

Detailed Description Text (6):
The plurality of pin heights as described hereinbefore work in conjunction with electronic circuitry to effect live insertion and removal, without damage to any electronic circuitry and without corruption of data. As illustrated in the block diagram of FIG. 2, insertion/removal logic 24 is required to sense or detect when a live insertion or removal is being undertaken, as indicated by circuitry on a sub-assembly being installed or removed. The insertion/removal logic 24 is resident on the processor board 13. The insertion/removal logic 24 communicates with bus arbitration logic 28 resident on the processor board 13. The bus arbitration logic, such as a VME bus arbiter known in the art, receives bus requests and prioritizes bus access. The known bus arbitration logic 28 is modified to accommodate a highest priority bus request which is issued by the insertion/removal logic 24 as discussed hereinafter.

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Detailed Description Text (7):
Referring now to FIGS. 2, 2a-2c and 3a, circuitry resident on the sub-assembly being inserted initiates signals which alert the insertion/removal logic 24 to a live insertion. Upon live insertion of a sub-assembly into the system, the long pins 18 make contact first and provide a reference or ground and a PRE.sub.-- VCC voltage of 5 volts. The PRE.sub.-- VCC 40 voltage biases a transistor T1 to issue an active low signal, LIFE.sub.-- PERIOD.sub.-- REQ.sub.-- L 42, which indicates that a live insertion is taking place. Preferrably, there are two LIFE.sub.-- PERIOD.sub.-- REQ.sub.-- L signals, one at either end of the connector or board, to assure issuance of the signal regardless of board skew or angle of insertion. The signals are appropriately terminated on the backplane and received by the insertion/removal logic 24 via schmidt trigger input and debounce circuitry (not shown) to account for any physical jitter during insertion. The signals are asserted from the time the long pins 18 contact until the short pins 22 contact and the board is fully seated.

Detailed Description Text (8):
The initial contact of the long pins 18 also biases open collector transistors T2 and T3, which illuminate an LED to indicate a live insertion period and issue an active low signal UNSEATED.sub.-- L 44, to indicate the sub-assembly is not yet seated, respectively.

Detailed Description Text (14):
Shortly thereafter, short pins 22 make contact and the sub-assembly or board is fully seated. The short pins 22, include Vcc pins which bypass the mosfet Q1 current limiting circuit. The mosfet Q1 internal resistance is bypassed when the VCC on short pins 22 makes contact. At this point the board voltage, VCC, reaches its maximum potential of +5 volts as shown in FIG. 3a. One of two short pins, preferrably located at opposing ends of the connector and designated LIFES.sub.-- BOARD.sub.-- INA.sub.-- L and LIFES.sub.-- BOARD.sub.-- INB.sub.-- L, is connected to ground on the sub-assembly inserted. The signals are connected together on the backplane and in combination result in a signal illustrated as LIFE.sub.-- BOARD.sub.-- IN.sub.-- L 60, shown in FIG. 3a. When the LIFE.sub.-- BOARD.sub.-- IN.sub.-- L 60 signal issues upon the two LIFES.sub.-- BOARD.sub.-- IN.sub.-- L signals being connected, the board is fully seated. The transistor T1 is turned off and the signal LIFE.sub.-- PERIOD.sub.-- REQ.sub.-- L 42 is deasserted. Upon recognizing LIFE.sub.-- PERIOD.sub.-- REQ.sub.-- L 42 is deasserted, the insertion/removal logic 24 deasserts the LIFE.sub.-- PERIOD.sub.-- IND signals and LIFE.sub.-- BUS.sub.-- REQ 25, and the live insertion is complete.

Detailed Description Text (15):
When a sub-assembly is removed from a live assembly or system, a process in reverse of that described hereinbefore effectively takes place. Referring now to FIGS. 2, 2a-2c and 3b, when either of the short pins generating LIFES.sub.-- BOARD.sub.-- IN.sub.-- L break contact, the ground pulling down and asserting LIFES.sub.-- BOARD.sub.-- INA.sub.-- L is lost and consequently LIFE.sub.-- PERIOD.sub.-- REQ.sub.-- L 42 is asserted via transistor T1 of FIG. 2a. At this point operation of the insertion/removal logic 24 and arbiter 28 is substantially as described hereinbefore with respect to insertion. Sub-assembly removal is complete when the LIFE.sub.-- PERIOD.sub.-- REQ.sub.-- L 42 signal or PRE.sub.-- VCC 40 break contact, whichever is first.

Detailed Description Text (31):
Although the invention is described as using sub-assembly resident transistor circuits and mosfet, it can be appreciated that other active switching devices such as e.g. bipolar transistors, Field Effect transistors, and time delay circuitry can be used, and could be backplane resident or located on other circuit boards.

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L3: Entry 23 of 28 File: USPT Apr 1, 1997

US-PAT-NO: 5617081
DOCUMENT-IDENTIFIER: US 5617081 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for live insertion and removal of electronic sub-assemblies

DATE-ISSUED: April 1, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Madnick; Jay L.	Derry	NH		
Hauser; Stephen A.	Burlington	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
3COM Corporation	Santa Clara	CA			02

APPL-NO: 08/ 398112 [PALM]
DATE FILED: March 3, 1995

PARENT-CASE:
RELATED APPLICATIONS This application is a division of U.S. patent application Ser. No. 08/191,391, filed Feb. 2, 1994, allowed U.S. Pat. No. 5,584,030 entitled: METHOD AND APPARATUS FOR LIVE INSERTION AND REMOVAL OF ELECTRONIC SUB-ASSEMBLIES, which is a divisional of Ser. No. 738,5581 filed Jul. 31, 1991 now U.S. Pat. No. 5,317,697, issued May 31, 1994, entitled: METHOD AND APPARATUS FOR LIVE INSERTION AND REMOVAL OF ELECTRONIC SUB-ASSEMBLIES.

INT-CL: [06] H04 Q 1/00

US-CL-ISSUED: 340/825.03; 340/825.16
US-CL-CURRENT: 710/302

FIELD-OF-SEARCH: 340/825.03, 340/825.05, 340/825.16, 340/825.07, 340/825.5, 340/825.52, 340/825.08, 395/282, 395/283, 395/281, 395/183.08, 370/85.5, 370/85.1, 370/85.13, 370/85.14

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

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☐	4527270	July 1985	Sweeton	371/11
☐	4775864	October 1988	Herman	340/825.5
☐	4803485	February 1989	Rypinski	340/825.05
☐	4835737	May 1989	Herrig et al.	364/900
☐	4905230	February 1990	Madge et al.	370/85.5
☐	4940969	July 1990	Taylor	340/653
☐	4956836	September 1990	Boatwright	370/16.1
☐	4999787	March 1991	McNally et al.	364/514
☐	5000531	March 1991	Burberry	350/96.16
☐	5115235	May 1992	Oliver	340/825.52
☐	5157771	October 1992	Losi et al.	395/325
☐	5210855	May 1993	Bartol	395/500
☐	5274800	December 1993	Babb et al.	395/183.08
☐	5287531	February 1994	Rogers, Jr. et al.	395/800
☐	5317697	May 1994	Husak et al.	395/283
☐	5408616	April 1995	Murr	395/281
☐	5471472	November 1995	McClure et al.	370/85.13

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
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139814	June 1986	JP	
192814	August 1987	JP	
251567	October 1989	JP	
73589	March 1990	JP	
164025	July 1991	JP	

ART-UNIT: 221

PRIMARY-EXAMINER: Holloway, III; Edwin C.

ATTY-AGENT-FIRM: Weingarten, Schurgin, Gagnebin & Hayes LLP

ABSTRACT:

A live insertion and removal mechanism assures that a sub-assembly being inserted or removed from a live electronic assembly does not disrupt system power and busses and is protected against the negative effects of current surge. Slot bypass circuitry is provided for effectively disconnecting selected output drivers from signal and control paths to avoid damage to the drivers upon insertion or removal of the sub-assembly from the live assembly.

3 Claims, 11 Drawing figures

L3: Entry 25 of 28 File: USPT Oct 22, 1996

DOCUMENT-IDENTIFIER: US 5568610 A
TITLE: Method and apparatus for detecting the insertion or removal of expansion cards using capacitive sensing

Brief Summary Text (20):
It is appreciated that an automatic detection method according to the present invention allows hot-swapping of expansion cards while system power remains on. This is particularly advantageous in server systems where it is very inconvenient to shut down the system to remove, insert, or otherwise replace expansion cards at the system level.

Detailed Description Text (10):
The control circuit 132 is preferably coupled to the data pins of the expansion card 101 for electrically isolating or tristating the data pins from remaining circuitry of the expansion card 101. Such isolation allows the data pins of the expansion card 101 to be electrically connected to the corresponding data pins of the connector 104 without data glitches. The control circuit 132 electrically connects the data pins of the expansion card 101 after it is inserted into the connector 104. Such signal isolation circuitry is implemented in any one of several known methods, such as the open collector of bipolar transistors or the high impedance current paths of field-effect transistors (FETs).

Detailed Description Text (11):
The power pins of the edge connector 102 are connected to one side of the current path of a transistor 134, which is preferably a field-effect transistor (FET). In particular, the drain of the FET 134 is connected to the power pins, where its source provides a signal PWR for providing power to various components of the expansion card 101 when the FET 134 is activated or turned on. The gate of the FET 134 receives an enable signal from a control circuit 132, which is further controlled by the processor 124. Several FETs connected in parallel may be necessary depending upon the power requirements of the expansion card 101 as well as heat dissipation considerations. Also, other electrically isolating devices could be used rather than one or more FETs. It is noted that the power pins of the expansion card 101 may be electrically isolated in the same manner as the data pins, except that one or more FETs are preferably used because of higher current needs of power pins.

CLAIMS:

27. The detection system of claim 26, wherein said control circuit includes a field-effect transistor for isolating said power pins of the I/O connector.

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L3: Entry 25 of 28 File: USPT Oct 22, 1996

US-PAT-NO: 5568610
DOCUMENT-IDENTIFIER: US 5568610 A

TITLE: Method and apparatus for detecting the insertion or removal of expansion cards using capacitive sensing

DATE-ISSUED: October 22, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brown; Alan E.	Georgetown	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dell USA, L.P.	Austin	TX			02

APPL-NO: 08/ 441485 [PALM]
DATE FILED: May 15, 1995

INT-CL: [06] G06 F 11/34

US-CL-ISSUED: 395/185.01; 395/282, 439/955
US-CL-CURRENT: 714/48; 439/955, 710/302

FIELD-OF-SEARCH: 395/180, 395/182.2, 395/325, 395/185.01, 395/282, 307/31, 307/66, 307/46, 307/85, 439/489, 439/911, 439/955

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4401358	August 1983	Daigaku	439/955
☐	4507697	March 1985	Ozil et al.	439/955
☐	4747783	May 1988	Bellamy et al.	439/59
☐	5021679	June 1991	Fairbanks et al.	307/66
☐	5184025	February 1993	McCurry et al.	307/66
☐	5287217	November 1993	Kobayashi et al.	265/228
☐	5317697	May 1994	Hurst et al.	395/325

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☐	5390081	February 1995	St. Pierre	361/775
☐	5432716	July 1995	Hahn et al.	395/325
☐	5451763	September 1995	Pickett et al.	235/492

ART-UNIT: 243

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Decady; Albert

ATTY-AGENT-FIRM: Garrana; Henry N. Kahler; Mark P. Turner; Michelle M.

ABSTRACT:

A detection system for detecting the insertion or removal of expansion cards having a standard edge connector using one or more capacitive plates coupled to corresponding variable frequency oscillators. The capacitive plates are preferably mounted on an internal layer of the expansion card and preferably aligned with corresponding pins of the edge connector for establishing capacitive loading with respect to the corresponding pins. The frequency of the oscillators change with changes in the capacitive loading of the corresponding plates. The detection circuitry includes a processor which continuously monitors the frequency of the oscillators to thereby detect movement of the expansion card, and preferably includes a control and isolation circuit which electrically isolates the power and data pins during insertion and/or removal as controlled by the processor. The detection circuitry may be mounted to either on the expansion card or the planar of the computer system. If mounted on the expansion card, the power and data pins are in a tristated condition while the option card is removed from the planar. The processor detects that the expansion card is being inserted or removed when the frequency of one or both oscillators is at a predetermined frequency or shifts by a predetermined amount.

28 Claims, 3 Drawing figures

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L3: Entry 26 of 28 File: USPT Jan 17, 1995

US-PAT-NO: 5383081
DOCUMENT-IDENTIFIER: US 5383081 A
** See image for Certificate of Correction **

TITLE: Live insertion circuit

DATE-ISSUED: January 17, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nishikawa; Naofumi	Hyogo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 08/ 185413 [PALM]
DATE FILED: January 24, 1994

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	5-029755	January 26, 1993

INT-CL: [06] H02 H 9/06

US-CL-ISSUED: 361/58; 361/110, 323/908, 336/DIG.2
US-CL-CURRENT: 361/58; 323/908, 336/DIG.2, 361/110

FIELD-OF-SEARCH: 361/58, 323/908, 336/DIG.2, 336/110, 336/136

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3995209	November 1976	Weston	336/DIG.2
☐	4405965	September 1983	Weldon et al.	361/58
☐	5153804	October 1992	Pham et al.	361/58

OTHER PUBLICATIONS

h e b b g e e e f c e b e ge

Katsuyuki Okada et al., "Physical Design Technologies for Network Node Processors", NTT R&D vol. 40, No. 10, 1991, pp. 1359-1370.

ART-UNIT: 214

PRIMARY-EXAMINER: DeBoer; Todd

ATTY-AGENT-FIRM: Rothwell, Figg, Ernst & Kurz

ABSTRACT:

The live insertion circuit of the present invention comprises a movable magnetic body for changing an inductance of a variable inductor, and the movable magnetic body is moved toward a supporting member by a rod at the time of inserting the package into the unit. At this time, an inductance of the variable inductor is changed according to the connection condition of terminals for connecting the package and the unit, thus suppressing a surge current.

14 Claims, 17 Drawing figures

First Hit Fwd Refs

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L3: Entry 27 of 28 File: USPT May 31, 1994

US-PAT-NO: 5317697
DOCUMENT-IDENTIFIER: US 5317697 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for live insertion and removal of electronic sub-assemblies

DATE-ISSUED: May 31, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Husak; David J.	Windham	NH		
Madnick; Jay L.	Derry	NH		
Hauser; Stephen A.	Burlington	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
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APPL-NO: 07/ 738581 [PALM]
DATE FILED: July 31, 1991

INT-CL: [05] G06F 13/20

US-CL-ISSUED: 395/325; 395/500, 395/DIG.1, 370/85.5
US-CL-CURRENT: 710/302; 370/217

FIELD-OF-SEARCH: 395/325, 395/500, 395/800, 370/161, 370/85.5

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4527270	July 1985	Sweeton	371/11
☐	4775864	October 1988	Herman	340/825.5
☐	4803485	February 1989	Rypinski	340/825.05
☐	4835737	May 1989	Herrig et al.	364/900
☐	4905230	February 1990	Madge et al.	370/85.5
☐	4940969	July 1990	Taylor	340/653

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☐	4956836	September 1990	Beatwright	370/16.1
☐	4999787	March 1991	McNally et al.	364/514
☐	5000531	March 1991	Burberry	350/96.16
☐	5157771	October 1992	Losi et al.	395/325
☐	5210855	May 1993	Bartol	395/500

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
90280	May 1984	JP	
139814	June 1986	JP	
192814	August 1987	JP	
251567	October 1989	JP	
73589	March 1990	JP	
164025	June 1991	JP	

ART-UNIT: 235

PRIMARY-EXAMINER: Lall; Parshotam S.

ASSISTANT-EXAMINER: Vu; Viet

ATTY-AGENT-FIRM: Weingarten, Schurgin, Gagnebin & Hayes

ABSTRACT:

A live insertion and removal mechanism assures that a sub-assembly being inserted or removed from a live electronic assembly does not disrupt system power and buses and is protected against the negative affects of current surge. An active current control device and related circuitry, and a connector having a plurality of graduated pin lengths effect a controlled ramp-up and ramp-down of power to the sub-assembly inserted into and removed from the live electronic assembly. Additionally, means are provided for effectively disconnecting selected output drivers from signal and control paths to avoid damage to the drivers upon insertion or removal of the sub-assembly from the live assembly.

29 Claims, 11 Drawing figures

US006614752B1

(12) **United States Patent**
Parrish et al.

(10) **Patent No.: US 6,614,752 B1**
(45) **Date of Patent: Sep. 2, 2003**

(54) **TRANSITIONING A STANDARDS-BASED CARD INTO A HIGH AVAILABILITY BACKPLANE ENVIRONMENT**

(75) Inventors: **Brent K. Parrish**, Hollis, NH (US); **Michael J. Taylor**, Pepperell, MA (US); **Michael P. Colton**, Deerville, NH (US)

(73) Assignee: **Cisco Technology, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/328,172**

(22) Filed: **Jun. 8, 1999**

(51) Int. Cl.[7] **H04L 12/24**

(52) U.S. Cl. **370/217**; 370/225; 714/2; 714/25

(58) Field of Search 370/217, 218, 370/219, 220, 221, 227, 243, 244, 245, 248, 249, 250, 251, 252, 225, 228; 340/825.06, 825.16; 714/2, 5, 10, 25, 30, 43, 44; 710/313, 314

(56) **References Cited**

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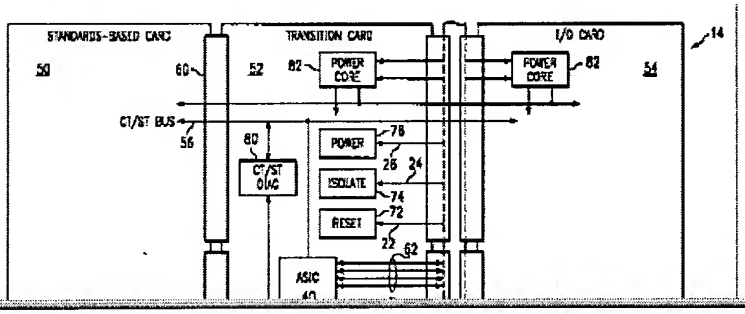
* cited by examiner

Primary Examiner—Steven Nguyen
Assistant Examiner—Duc Duong
(74) *Attorney, Agent, or Firm*—Baker Botts L.L.P.

(57) **ABSTRACT**

A telecommunications device includes a backplane having an associated high availability backplane environment. A transition card coupled to the backplane helps transition a standards-based card supporting a Peripheral Component Interconnect (PCI) administrative bus into the high availability backplane environment. The transition card may also help transition either a Computer Telephony or a Serial Telephony serial data bus into the high availability backplane environment. In a more particular embodiment, the transition card may support a control bus, a synchronization bus, a reset bus, an isolate bus, and a power bus that each support at least one high availability characteristic not associated with the PCI bus. In another more particular embodiment, the transition card may provide at least some redundancy, hot insertion, fault detection, fault isolation, and fault recovery capabilities not associated with the PCI bus.

41 Claims, 3 Drawing Sheets



US-PAT-NO: 6614752

DOCUMENT-IDENTIFIER: US 6614752 B1
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TITLE: Transitioning a standards-based card into a high availability backplane environment

---------- KWIC ---------

Detailed Description Text - DETX (22):
Control bus 18 also supports hot insertion of switching unit controllers 12 and service providers 14 during operation of switching unit 10, using appropriate isolation integrated circuits or otherwise. As a result of these and other features, described more fully in copending U.S. application Ser. No. 09/328,171 and U.S. Pat. No. 6,425,009 control bus 18 prevents single points of failure from propagating within switching unit 10 and helps satisfy high availability requirements. Advantages of control bus 18 are particularly apparent in contrast to bus 58, which is prone to single points of failure and does not provide an acceptable combination of redundancy, hot insertion, and fault detection, isolation, and recovery capabilities. Transition card 52 provides a bridge between bus 58 and control bus 18, allowing switching unit controllers 12 and service providers 14 to communicate suitable command, control, and administrative information within the high availability backplane environment associated with backplane 16.

Detailed Description Text - DETX (28):
Synchronization bus 20 also supports hot insertion of switching unit controllers 12 and service providers 14 during operation of switching unit 10, using appropriate isolation integrated circuits or otherwise. As a result of these and other features, as described more fully in copending U.S. application Ser. Nos. 09/328,031 and 09/330,433, synchronization bus 20 prevents single points of failure from propagating and helps to satisfy high availability requirements. The advantages of synchronization bus 20 are particularly apparent in contrast to buses 56 and 58, which are both prone to single points of failure and do not provide a suitable combination of redundancy, hot insertion, and fault detection, isolation, and recovery capabilities. In general, transition card 52 takes redundant frame pulses and

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Search Results - Record(s) 1 through 10 of 11 returned.

☐ 1. Document ID: US 6343207 B1

L1: Entry 1 of 11 File: USPT Jan 29, 2002

US-PAT-NO: 6343207
DOCUMENT-IDENTIFIER: US 6343207 B1

TITLE: Field programmable radio frequency communications equipment including a configurable if circuit, and method therefor

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 2. Document ID: US 6282627 B1

L1: Entry 2 of 11 File: USPT Aug 28, 2001

US-PAT-NO: 6282627
DOCUMENT-IDENTIFIER: US 6282627 B1

TITLE: Integrated processor and programmable data path chip for reconfigurable computing

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 3. Document ID: US 6279045 B1

L1: Entry 3 of 11 File: USPT Aug 21, 2001

US-PAT-NO: 6279045
DOCUMENT-IDENTIFIER: US 6279045 B1

TITLE: Multimedia interface having a multimedia processor and a field programmable gate array

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 4. Document ID: US 6096091 A

L1: Entry 4 of 11 File: USPT Aug 1, 2000

h e b b g e e e f e ef b e

US-PAT-NO: 6096091
DOCUMENT-IDENTIFIER: US 6096091 A
** See image for Certificate of Correction **

TITLE: Dynamically reconfigurable logic networks interconnected by fall-through FIFOs for flexible pipeline processing in a system-on-a-chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6020755 A

L1: Entry 5 of 11 File: USPT Feb 1, 2000

US-PAT-NO: 6020755
DOCUMENT-IDENTIFIER: US 6020755 A

TITLE: Hybrid programmable gate arrays

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5970254 A

L1: Entry 6 of 11 File: USPT Oct 19, 1999

US-PAT-NO: 5970254
DOCUMENT-IDENTIFIER: US 5970254 A

TITLE: Integrated processor and programmable data path chip for reconfigurable computing

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5752035 A

L1: Entry 7 of 11 File: USPT May 12, 1998

US-PAT-NO: 5752035
DOCUMENT-IDENTIFIER: US 5752035 A

TITLE: Method for compiling and executing programs for reprogrammable instruction set accelerator

Full | Title | Citation | Front | Review | Classification | Date | Reference | ... | Claims | KWIC | Draw De

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☐ 8. Document ID: US 5671355 A

L1: Entry 8 of 11 File: USPT Sep 23, 1997

US-PAT-NO: 5671355
DOCUMENT-IDENTIFIER: US 5671355 A

h e b b g e e e f e ef b e

TITLE: Reconfigurable network interface apparatus and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 9. Document ID: US 5652904 A

L1: Entry 9 of 11 File: USPT Jul 29, 1997

US-PAT-NO: 5652904
DOCUMENT-IDENTIFIER: US 5652904 A
**** See image for Certificate of Correction ****

TITLE: Non-reconfigurable microprocessor-emulated FPGA

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 10. Document ID: US 5537601 A

L1: Entry 10 of 11 File: USPT Jul 16, 1996

US-PAT-NO: 5537601
DOCUMENT-IDENTIFIER: US 5537601 A

TITLE: Programmable digital signal processor for performing a plurality of signal processings

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

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Terms	Documents
5361373.pn. or 5537601.pn. or 5652904.pn. or 5671355.pn. or 5752035.pn. or 5970254.pn. or 6020755.pn. or 6096091.pn. or 6279045.pn. or 6282627.pn. or 6343207.pn.	11

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